

FIG. 1

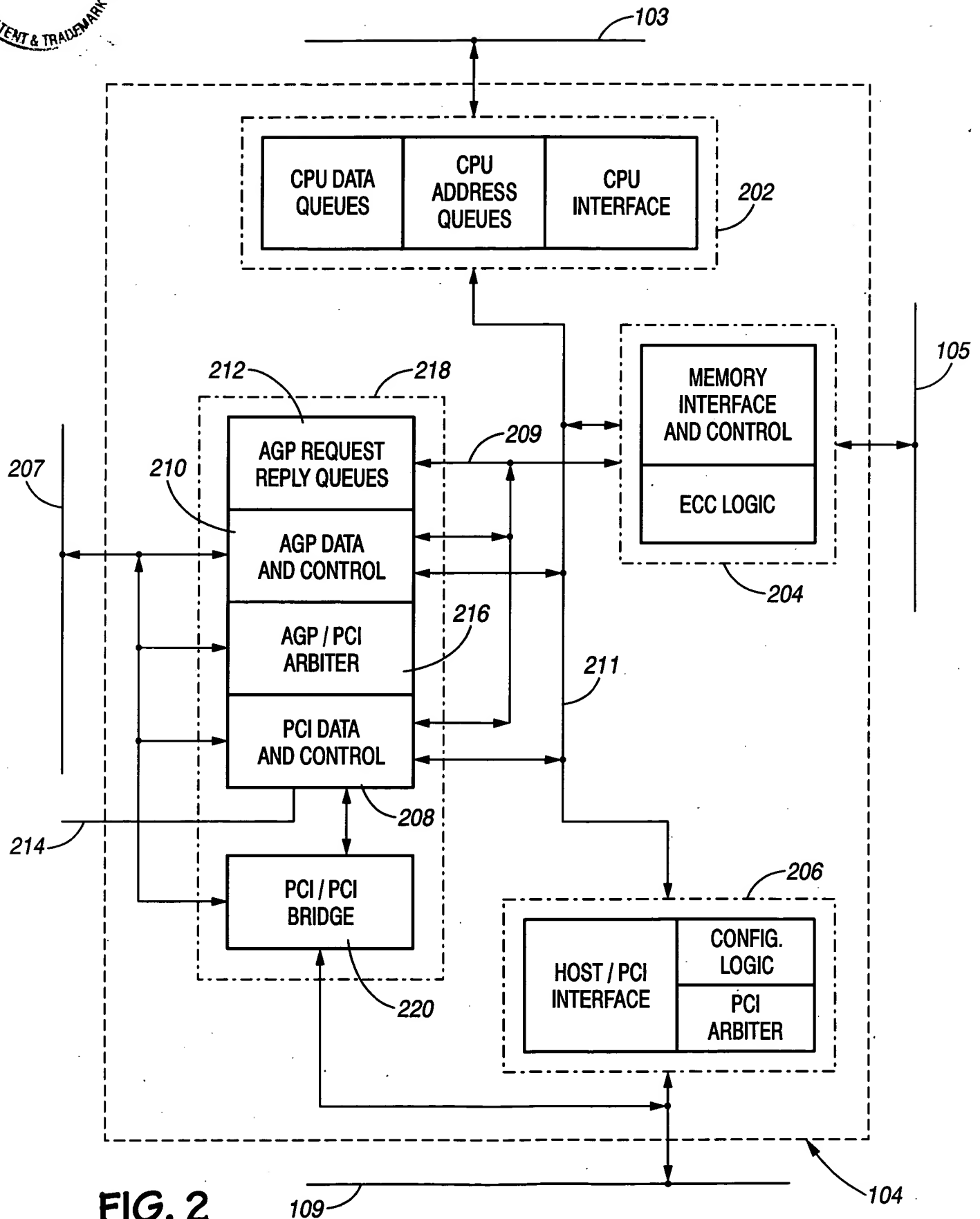


FIG. 2

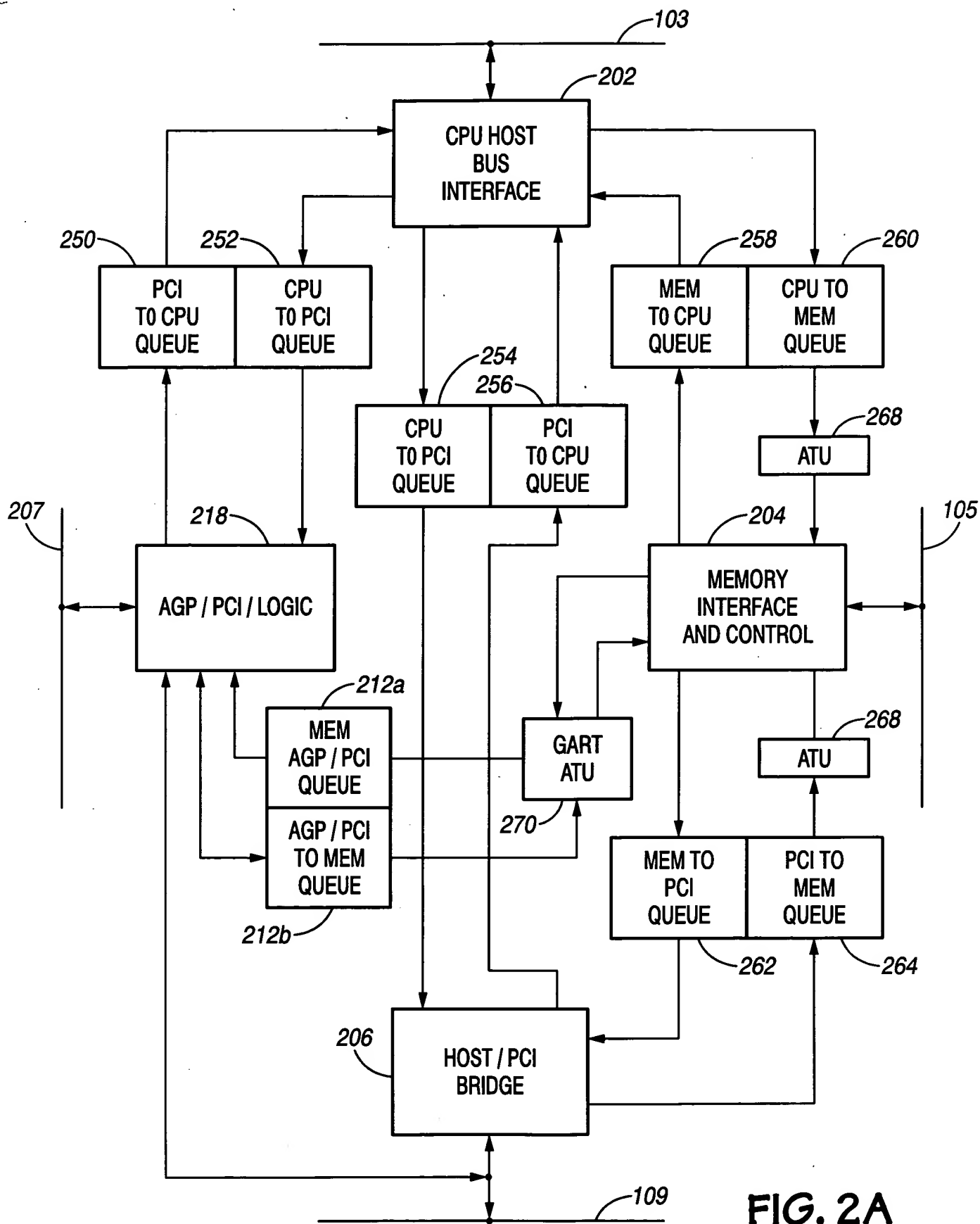


FIG. 2A

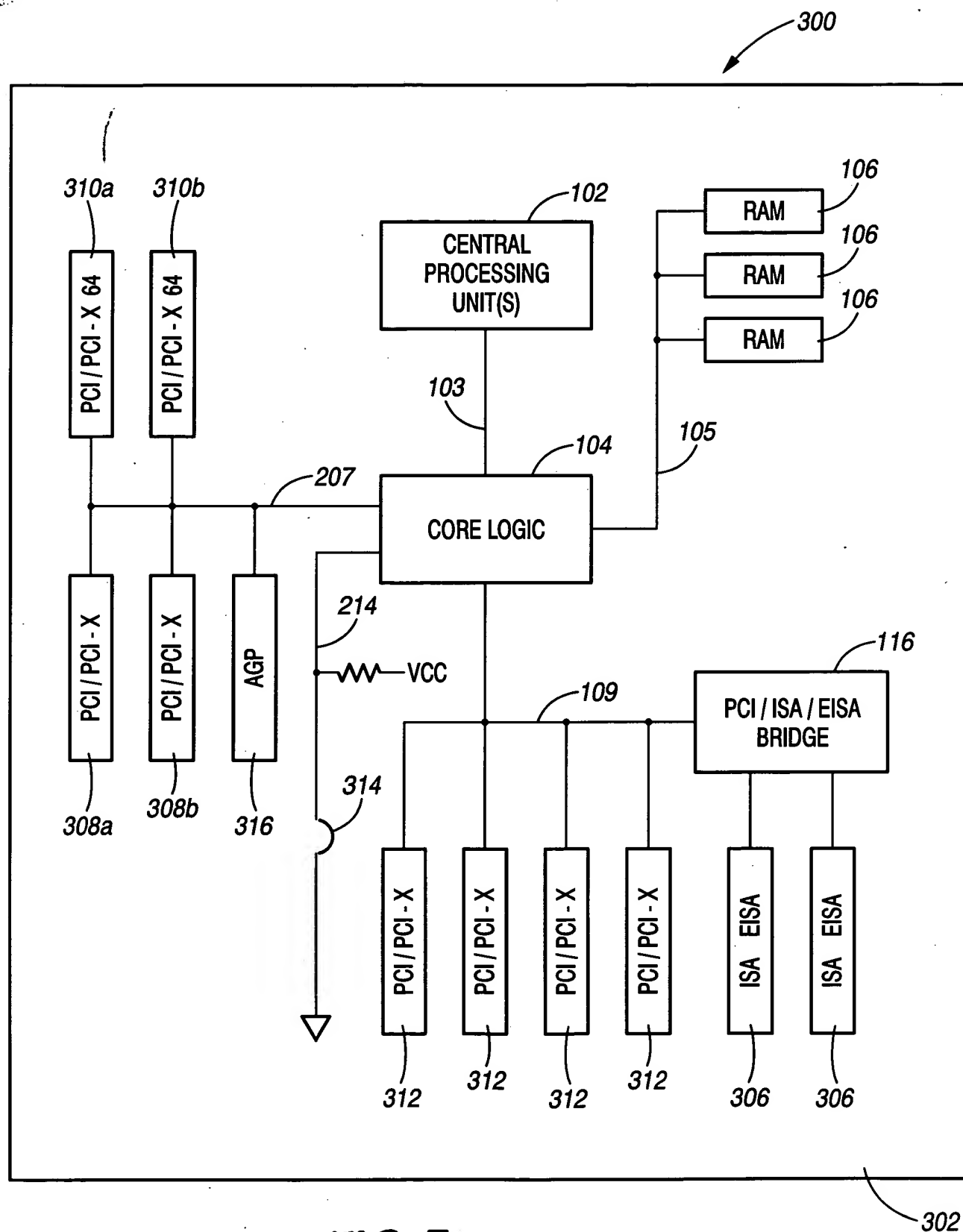


FIG. 3

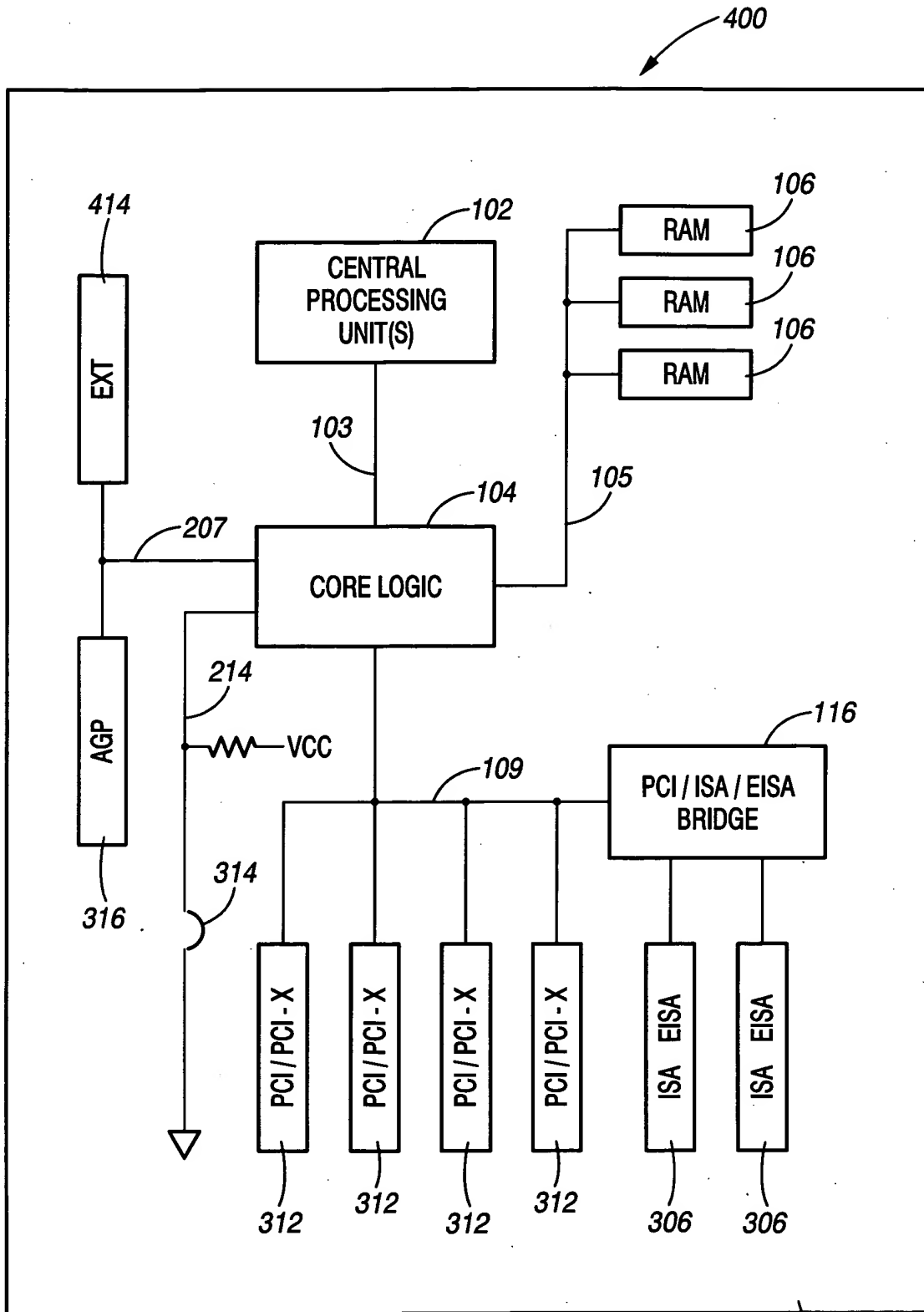


FIG. 4

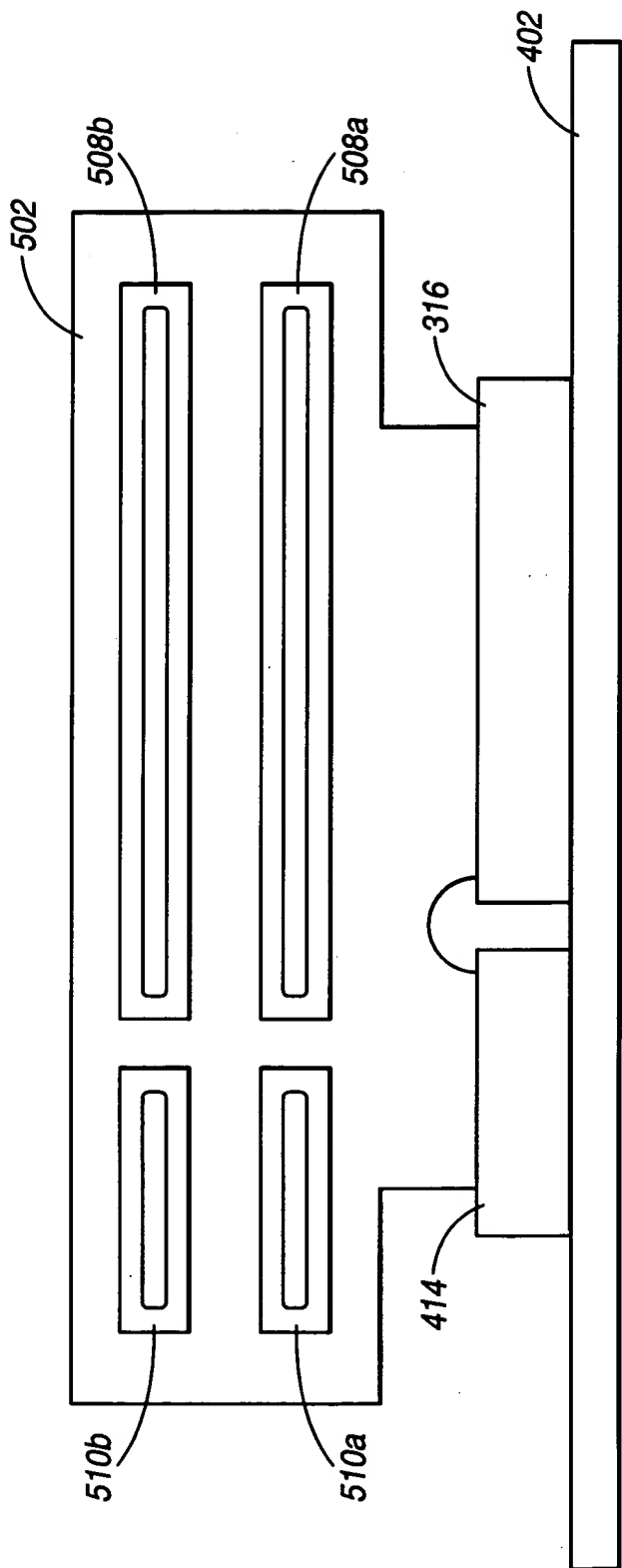


FIG. 5

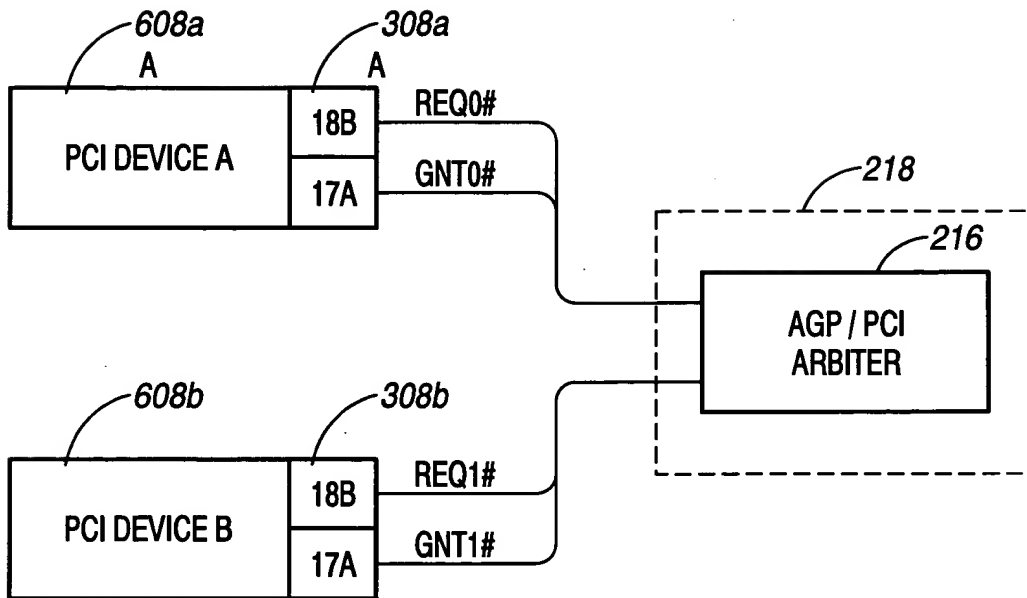
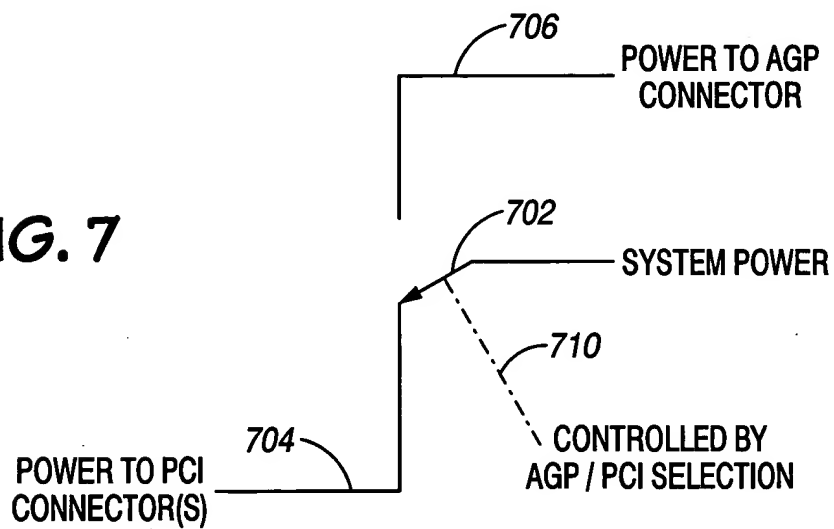


FIG. 6

FIG. 7



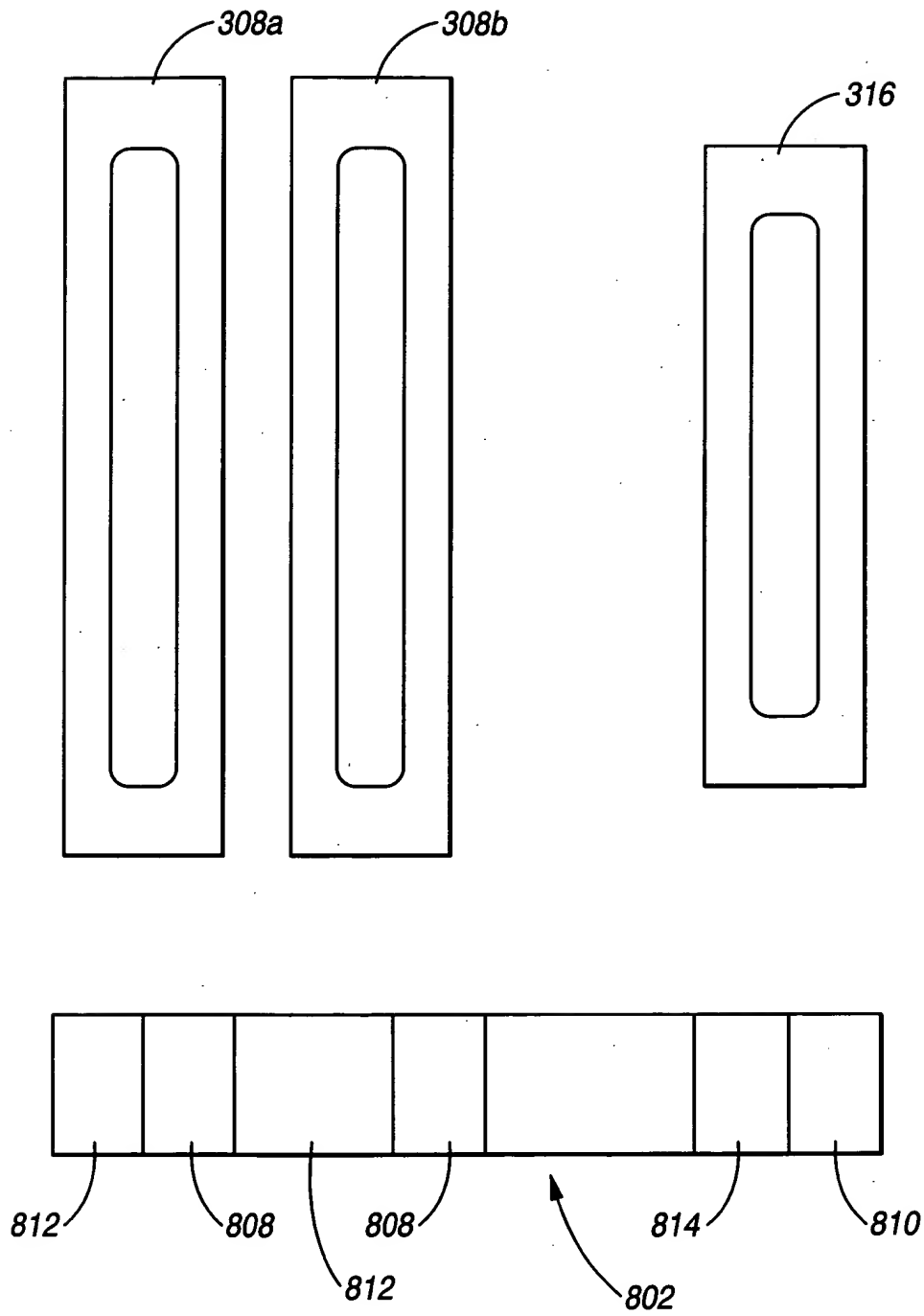


FIG. 8A

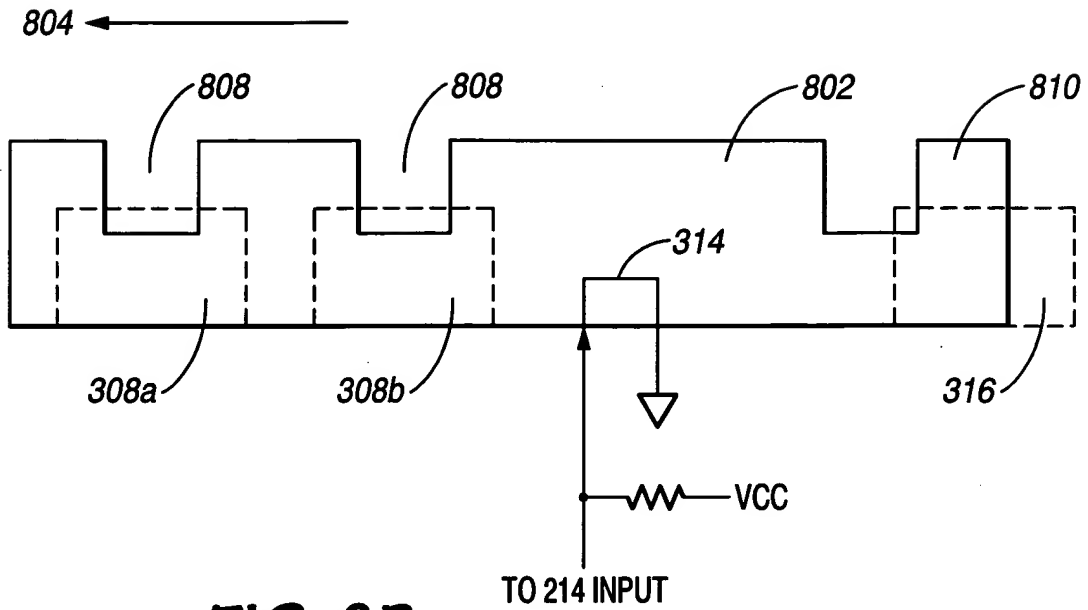


FIG. 8B

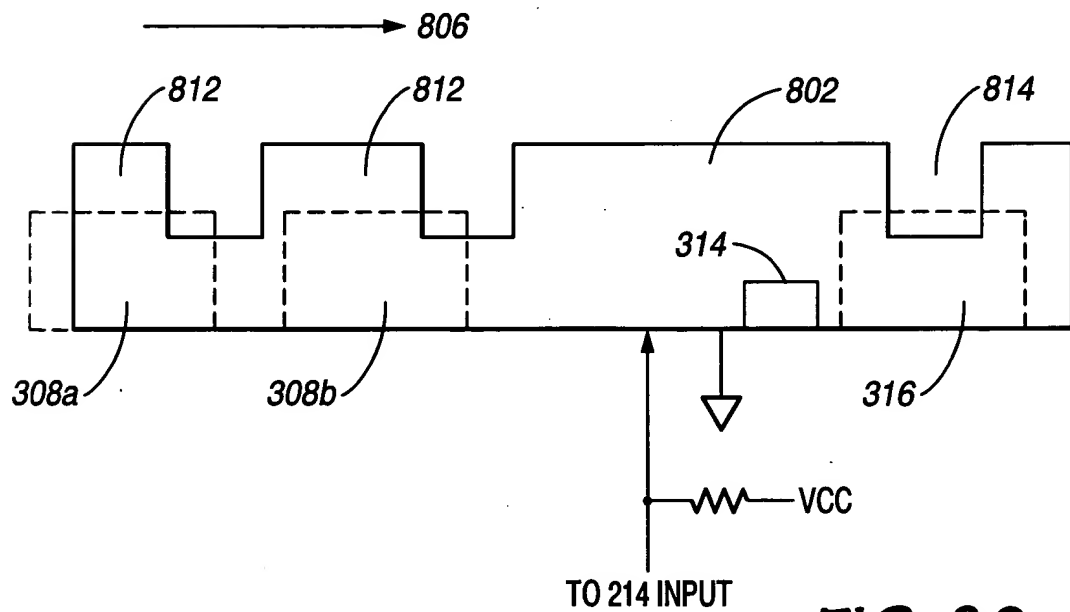


FIG. 8C

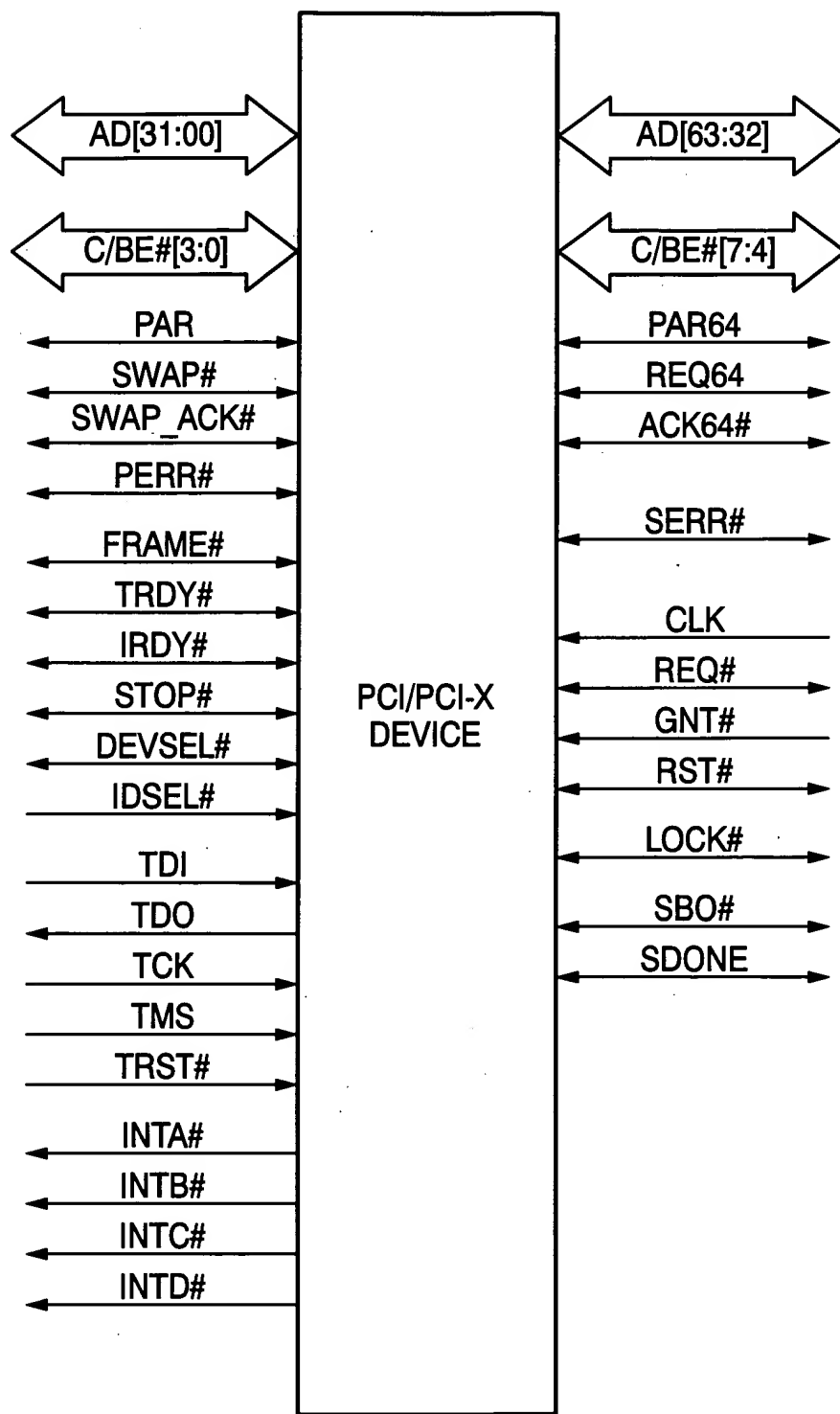


FIG. 9

Byte 3		Byte 2		Byte 1		Byte 0		
Device ID				Vendor ID				00h
Status				Command				04h
Class Code						Revision ID		08h
Bist		Header Type		Latency Timer		Cache Line Size		0Ch
Base Address Registers								10h
								14h
								18h
								1Ch
								20h
Cardbus CIS Pointer								24h
								28h
Subsystem ID				Subsystem Vendor ID				2Ch
Expansion ROM Base Address								30h
Reserved								34h
Reserved								38h
Max_Lat		Min_GNT		Inter. Pin		Inter. Line		3Ch

FIG. 10

1000

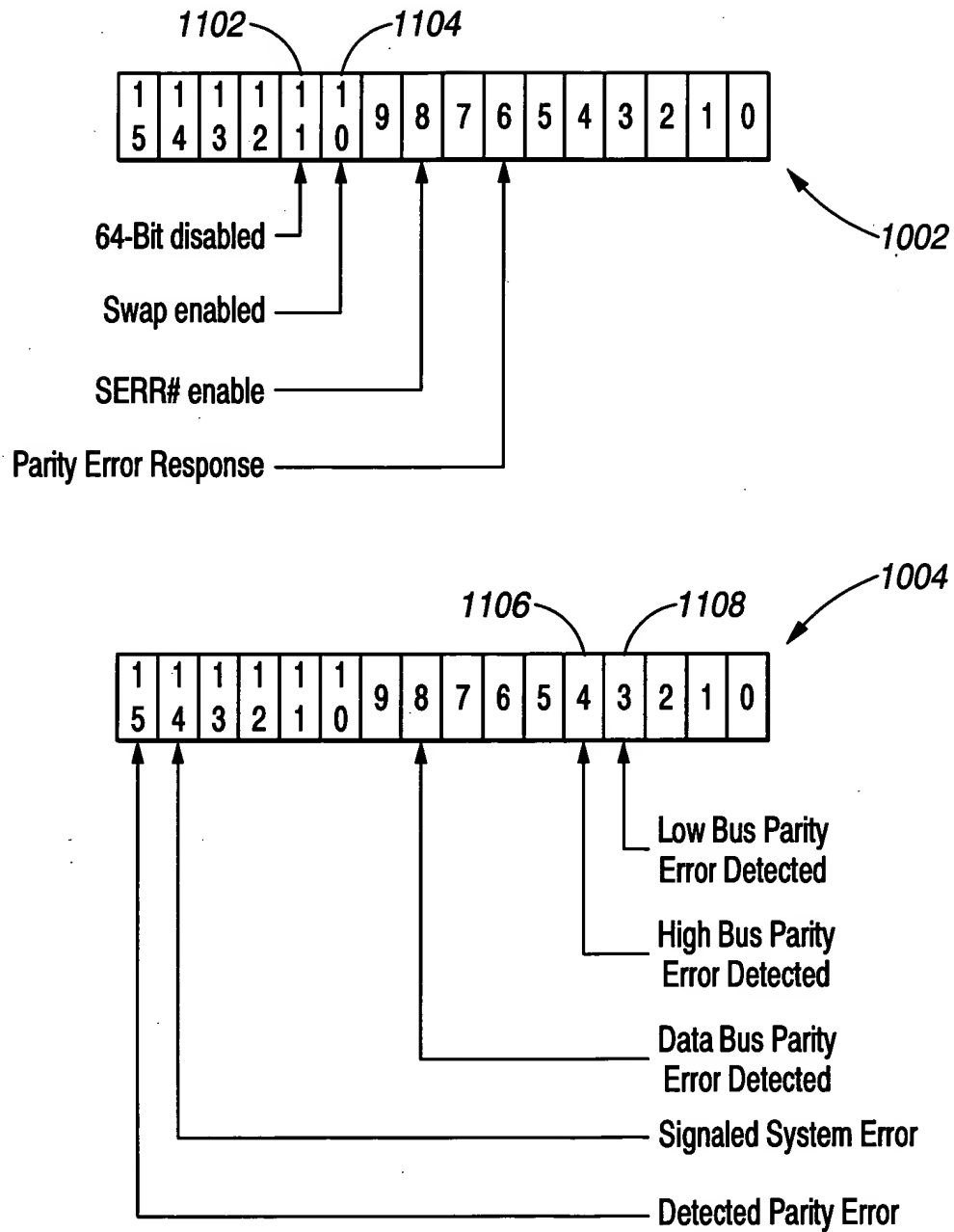


FIG. 11

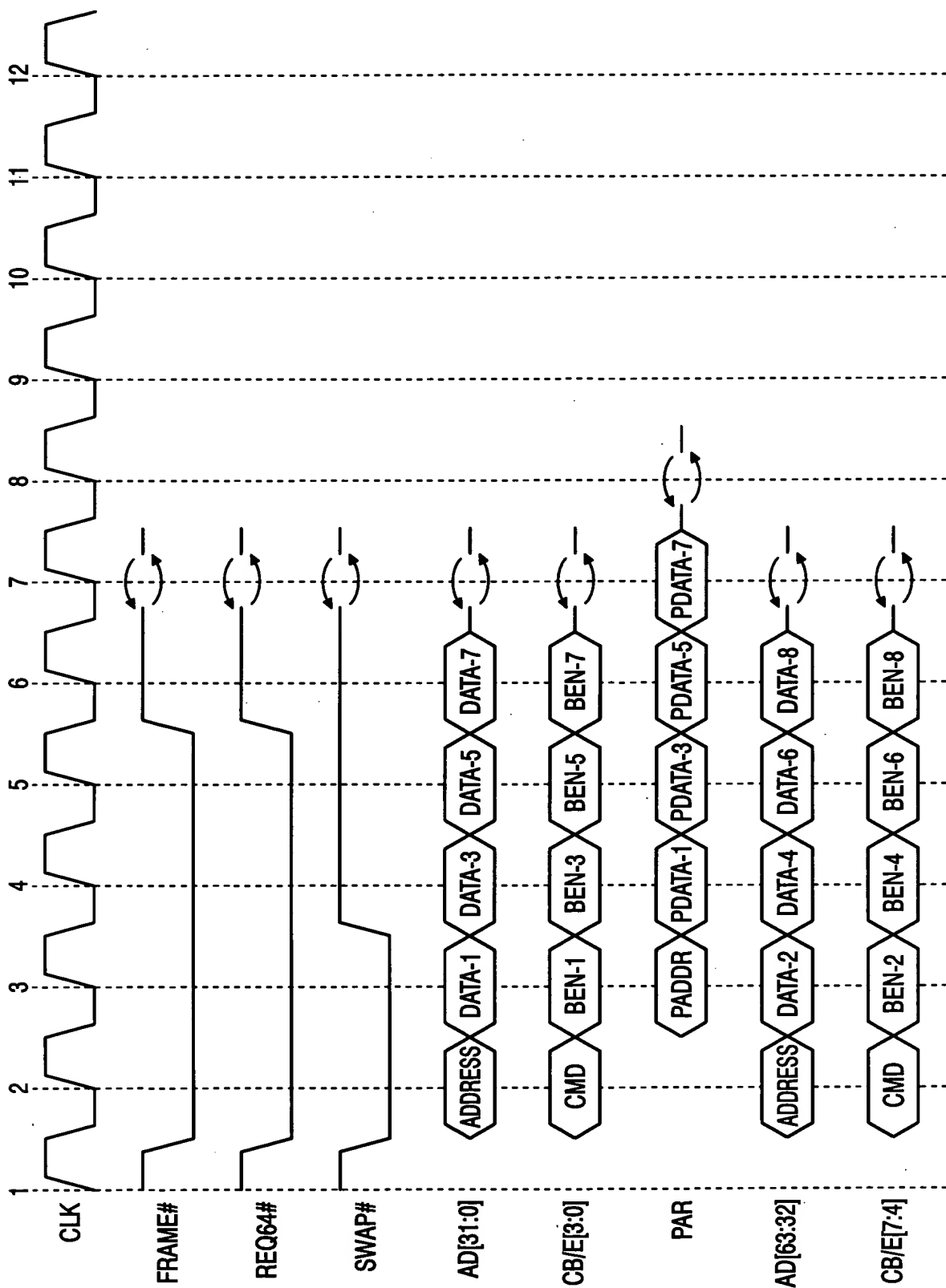


FIG. 12A

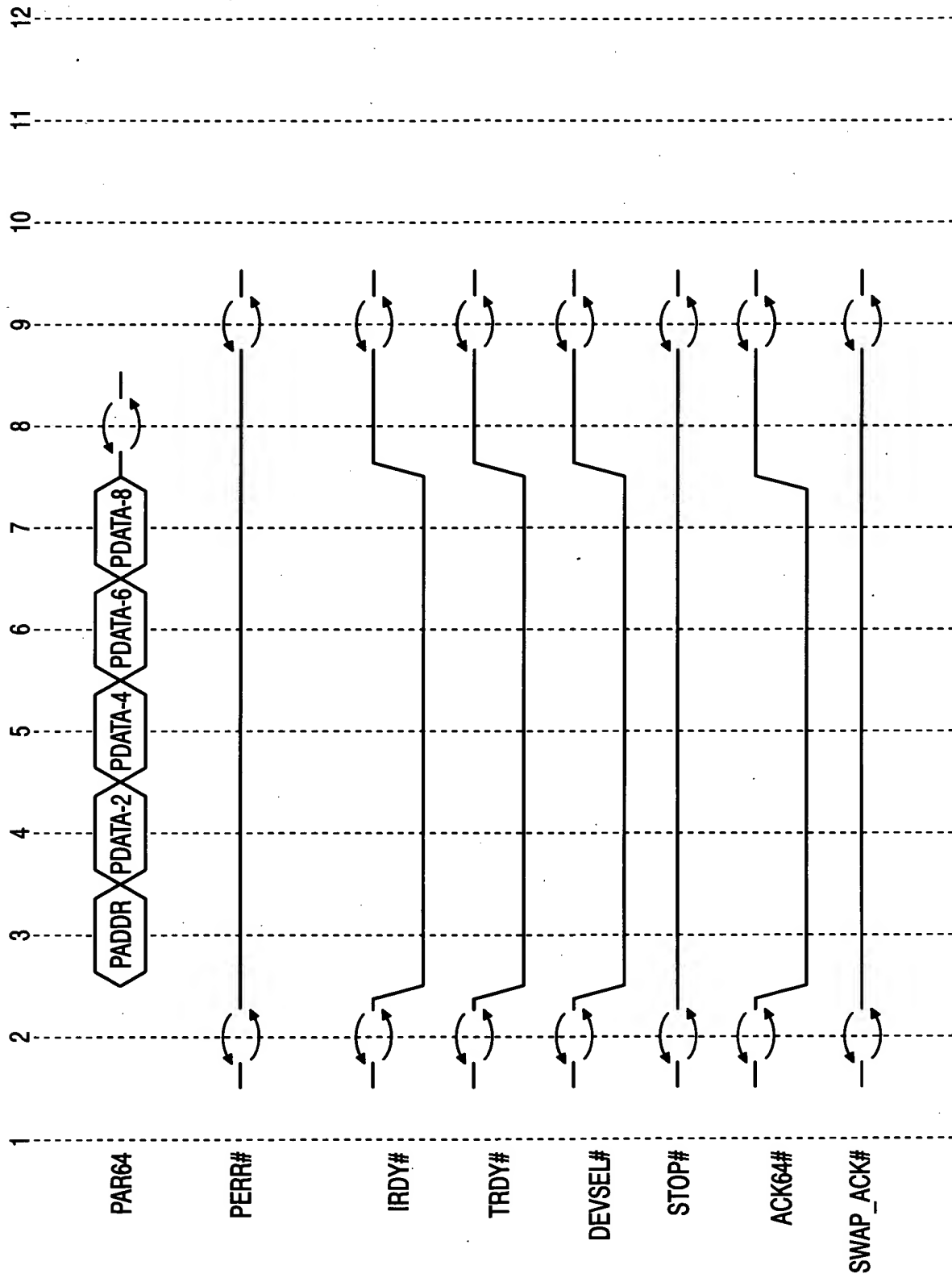


FIG. 12B

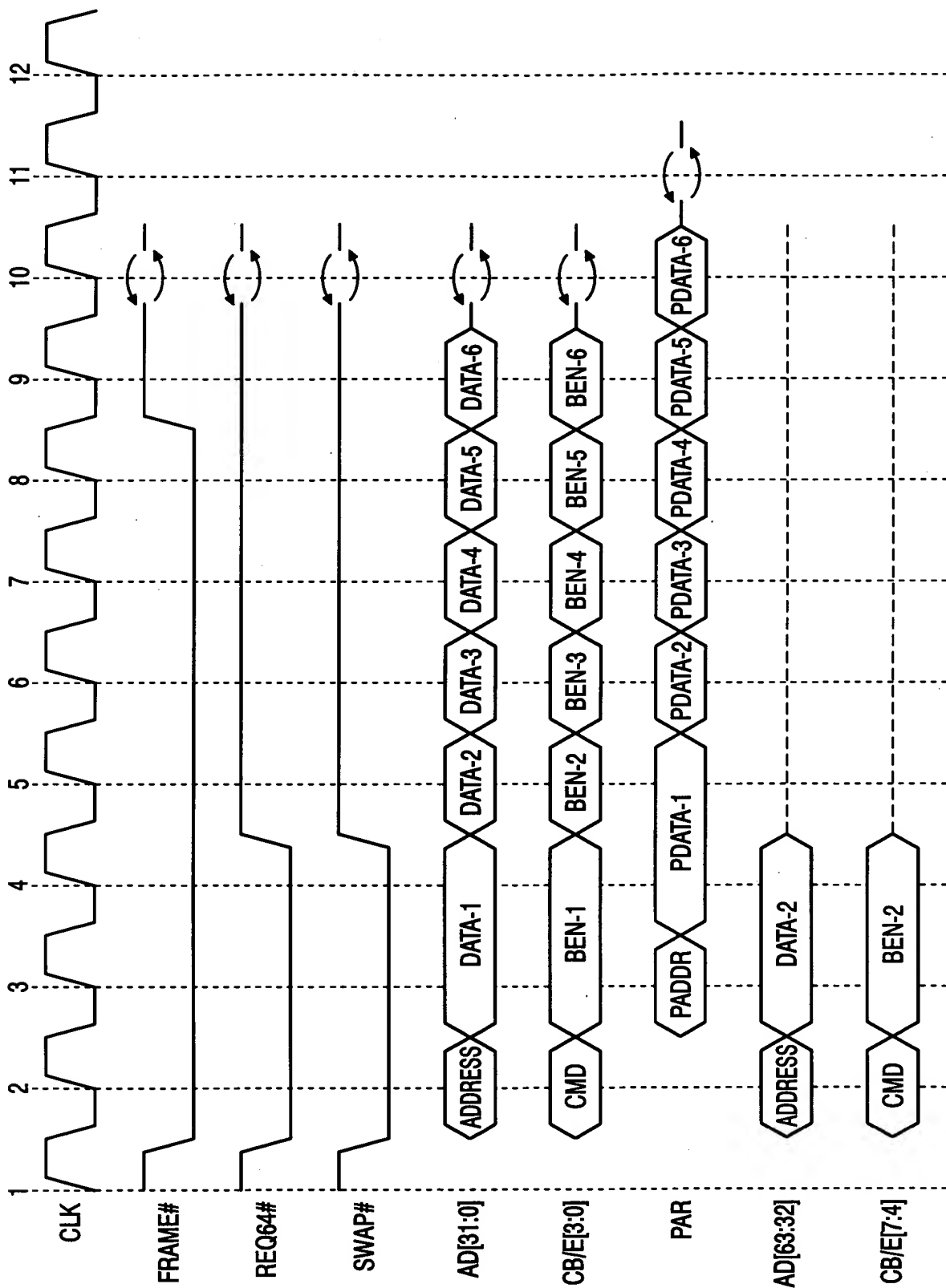


FIG. 13A

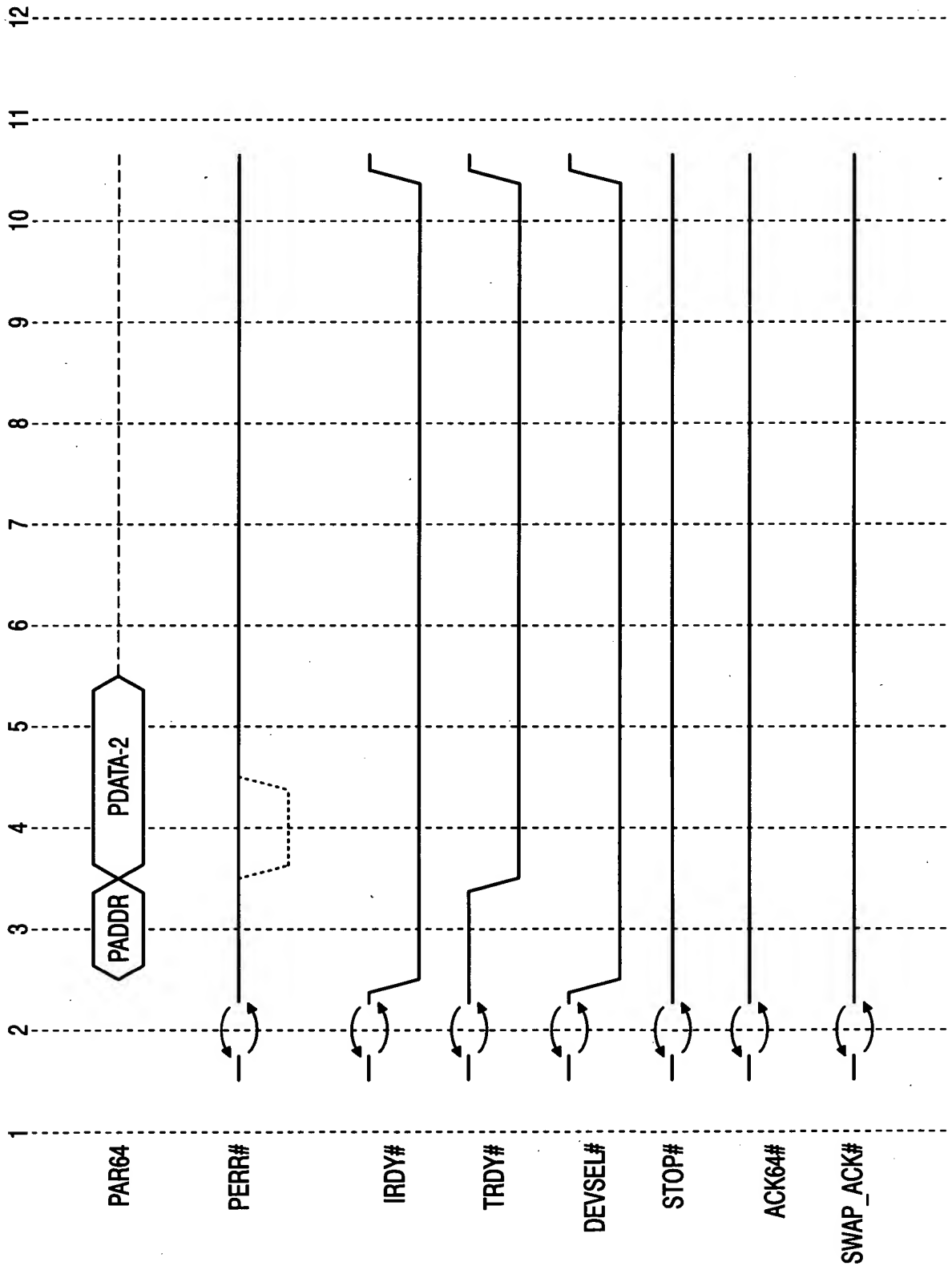


FIG. 13B

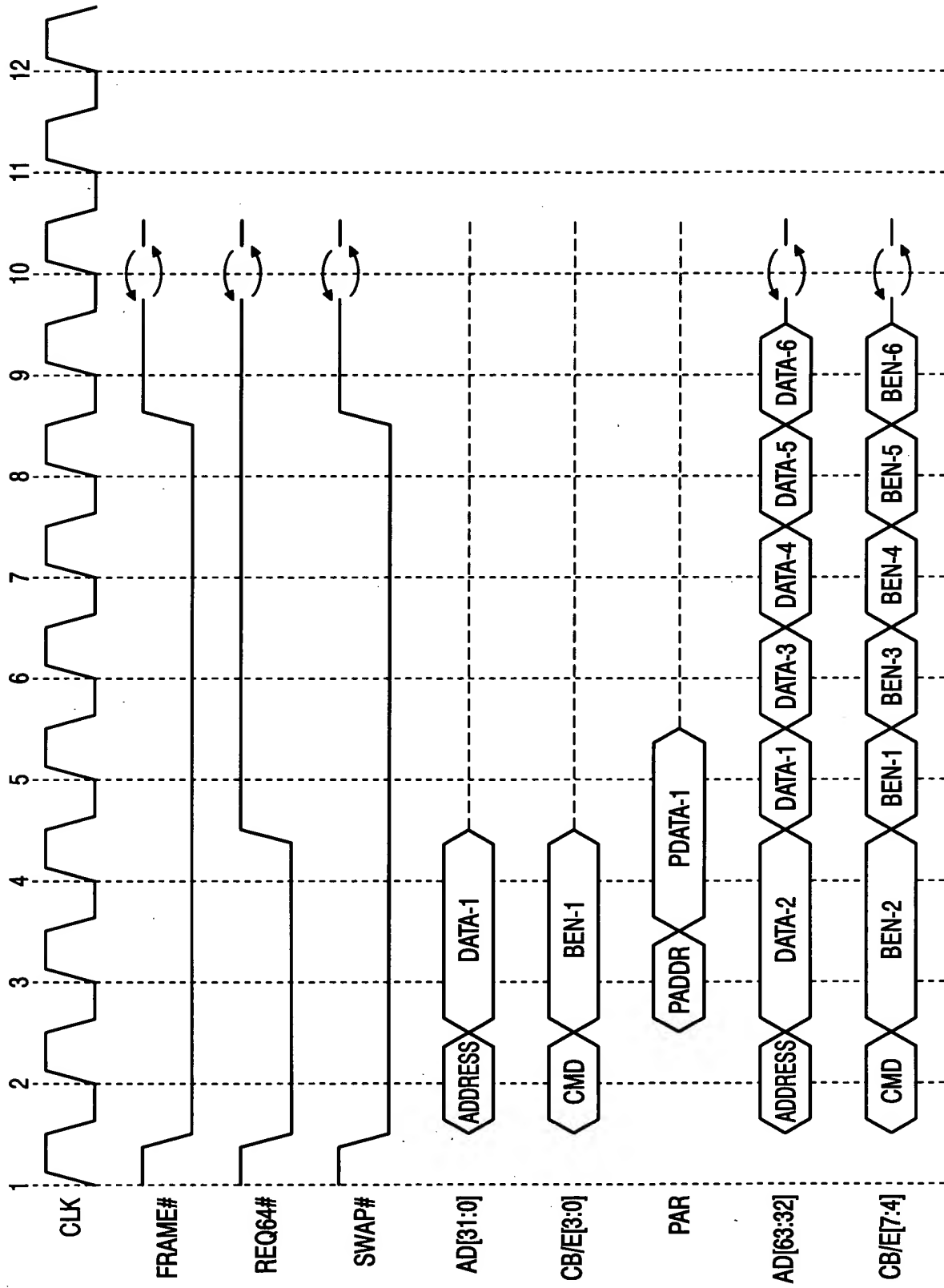


FIG. 14A

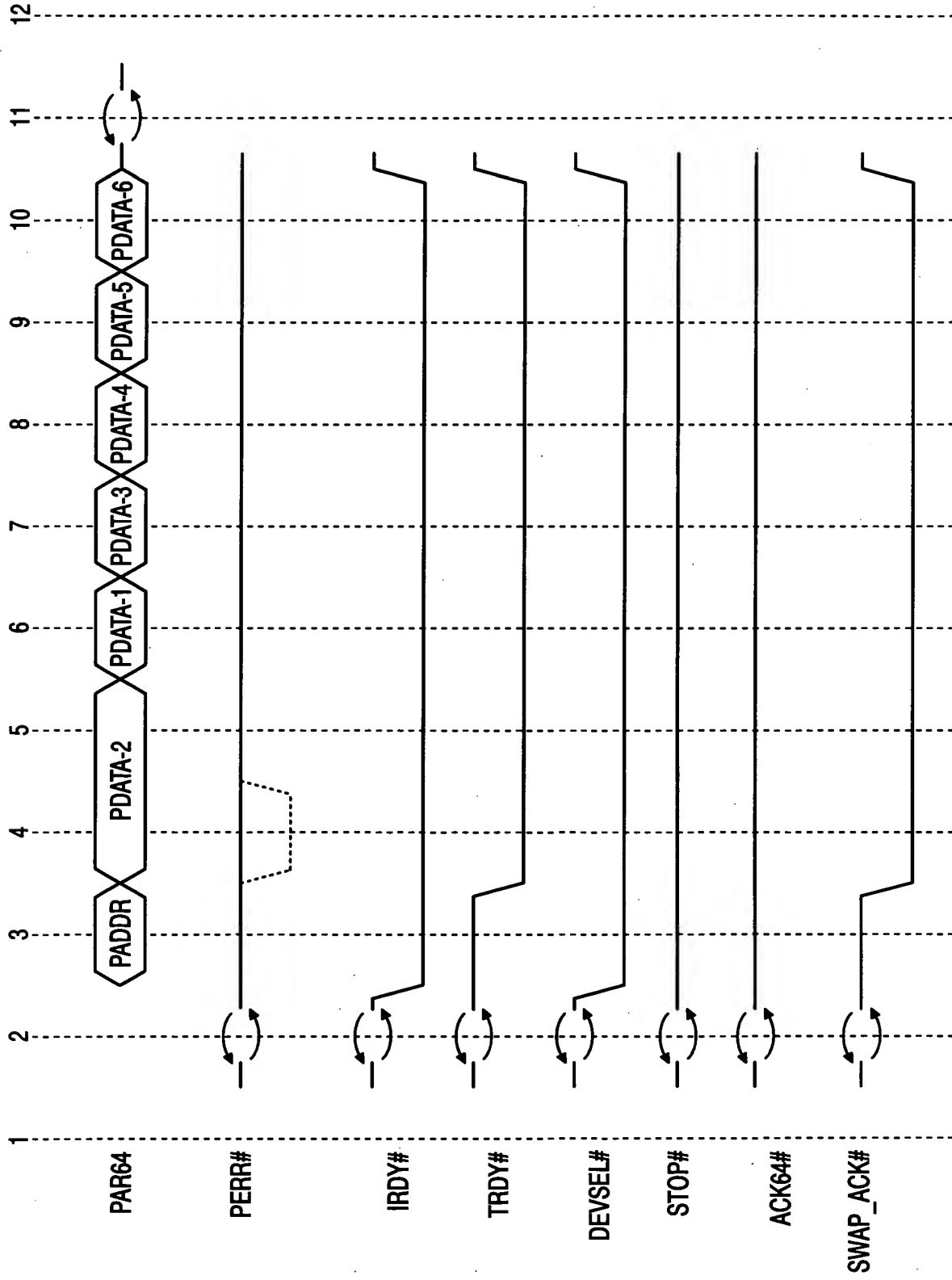


FIG. 14B

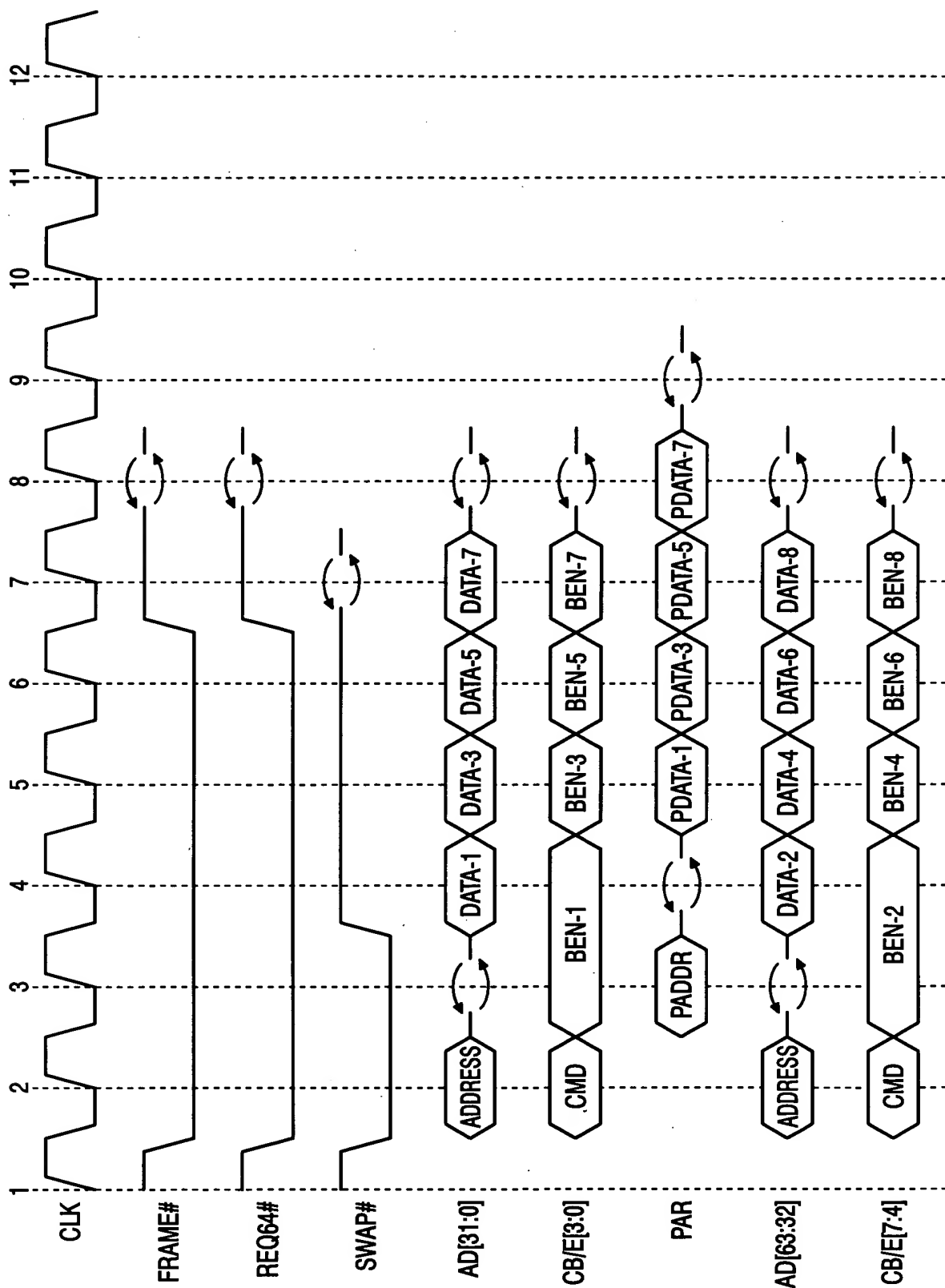


FIG. 15A

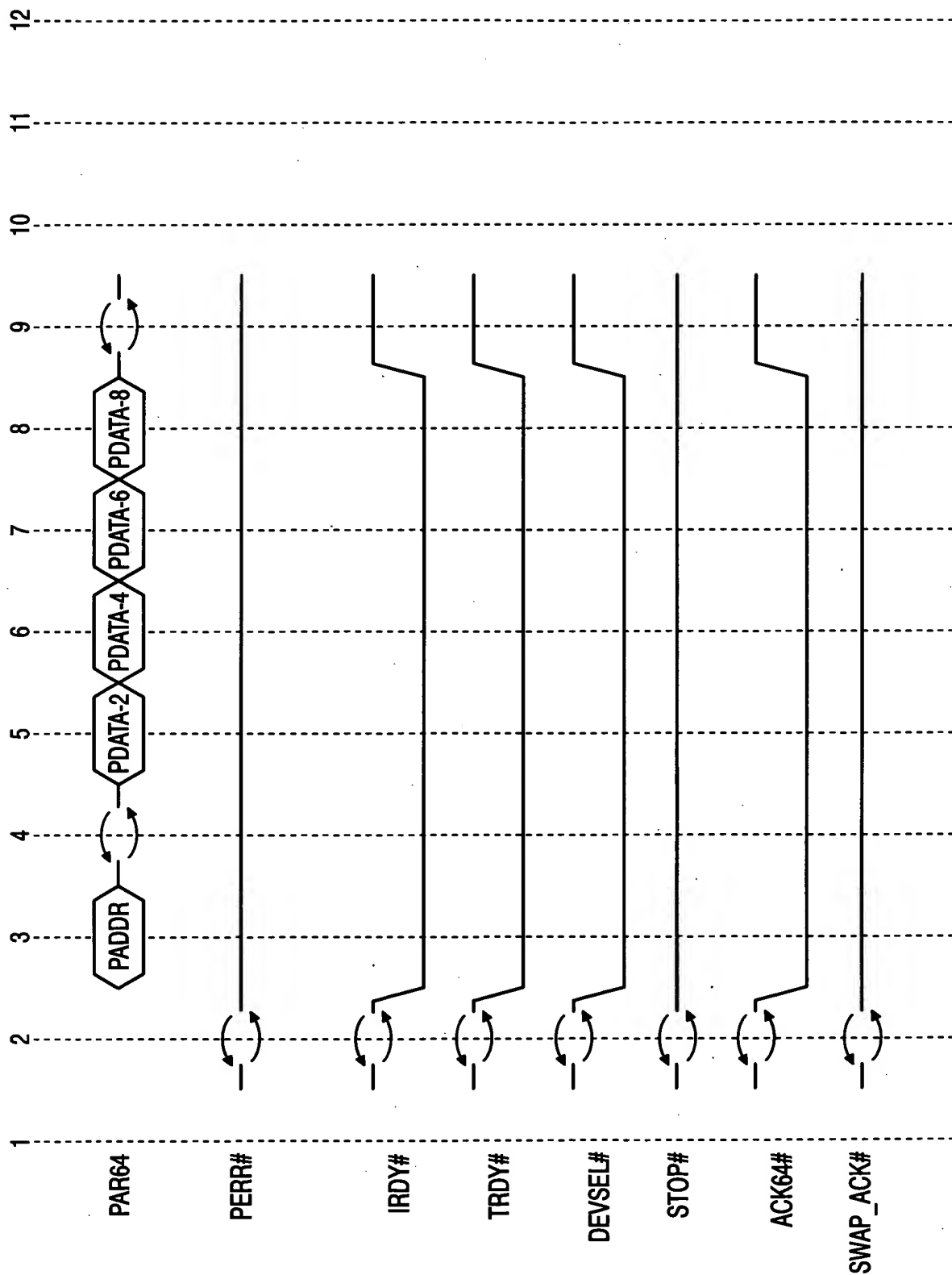


FIG. 15B

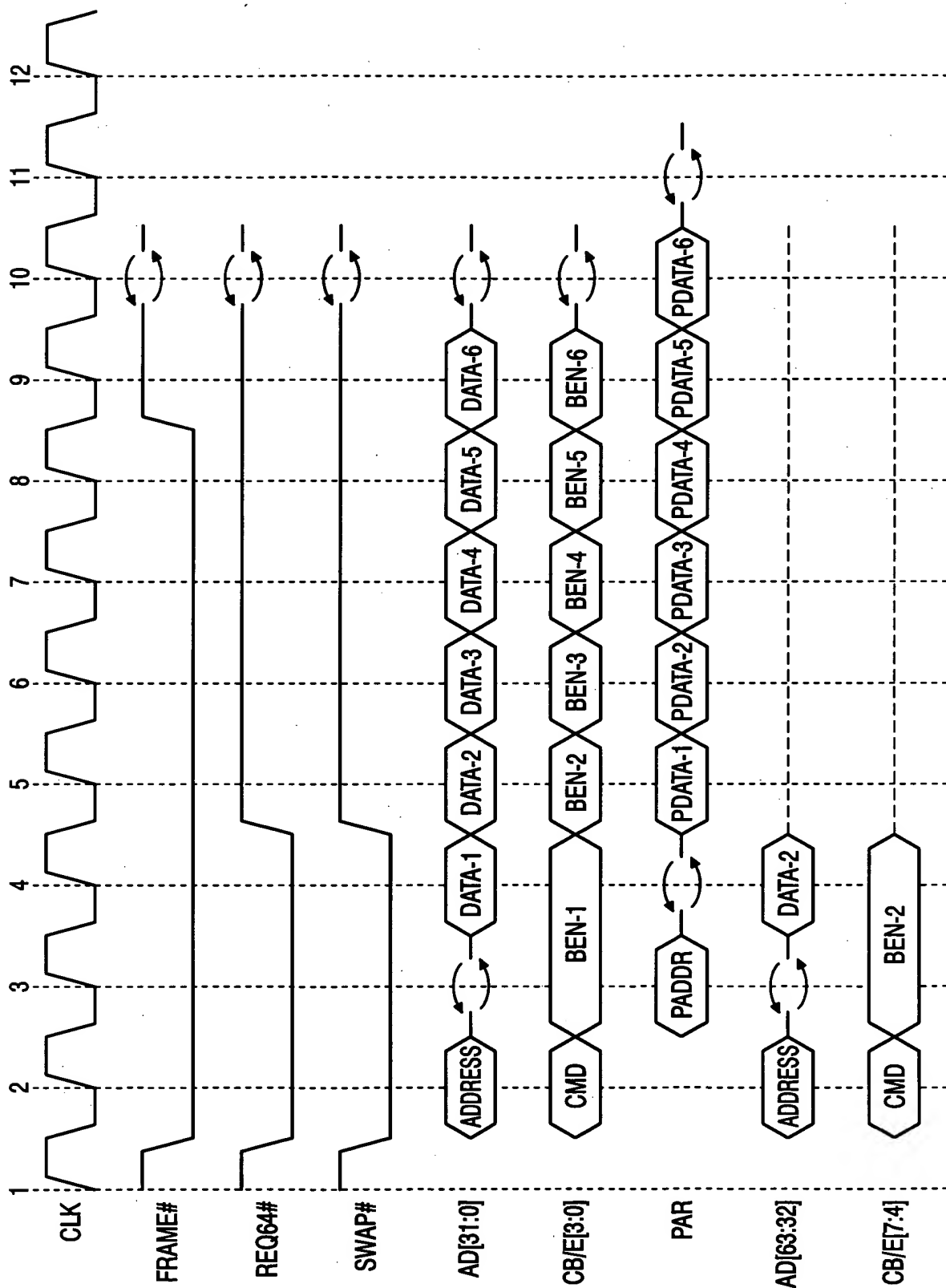


FIG. 16A

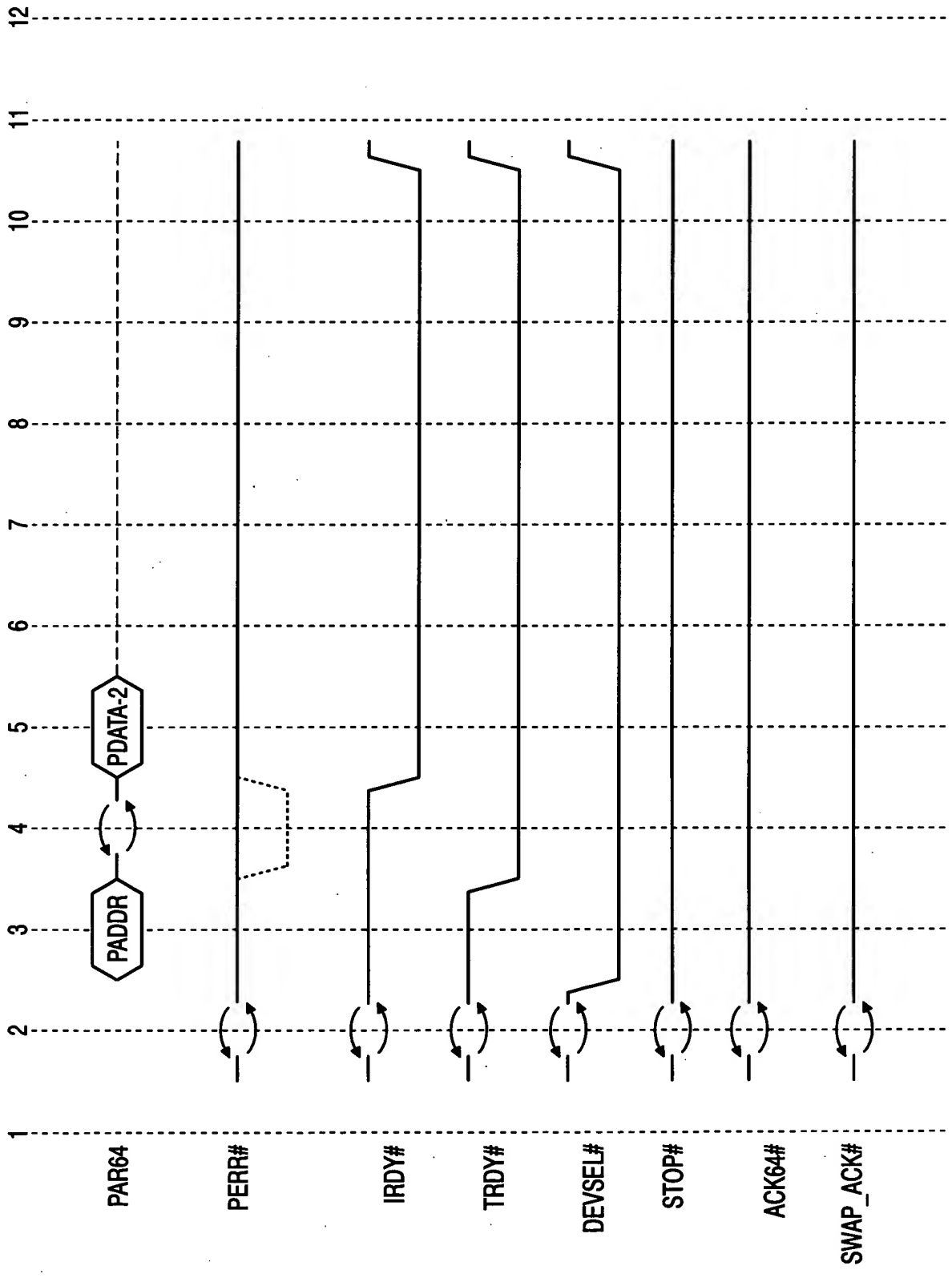


FIG. 16B

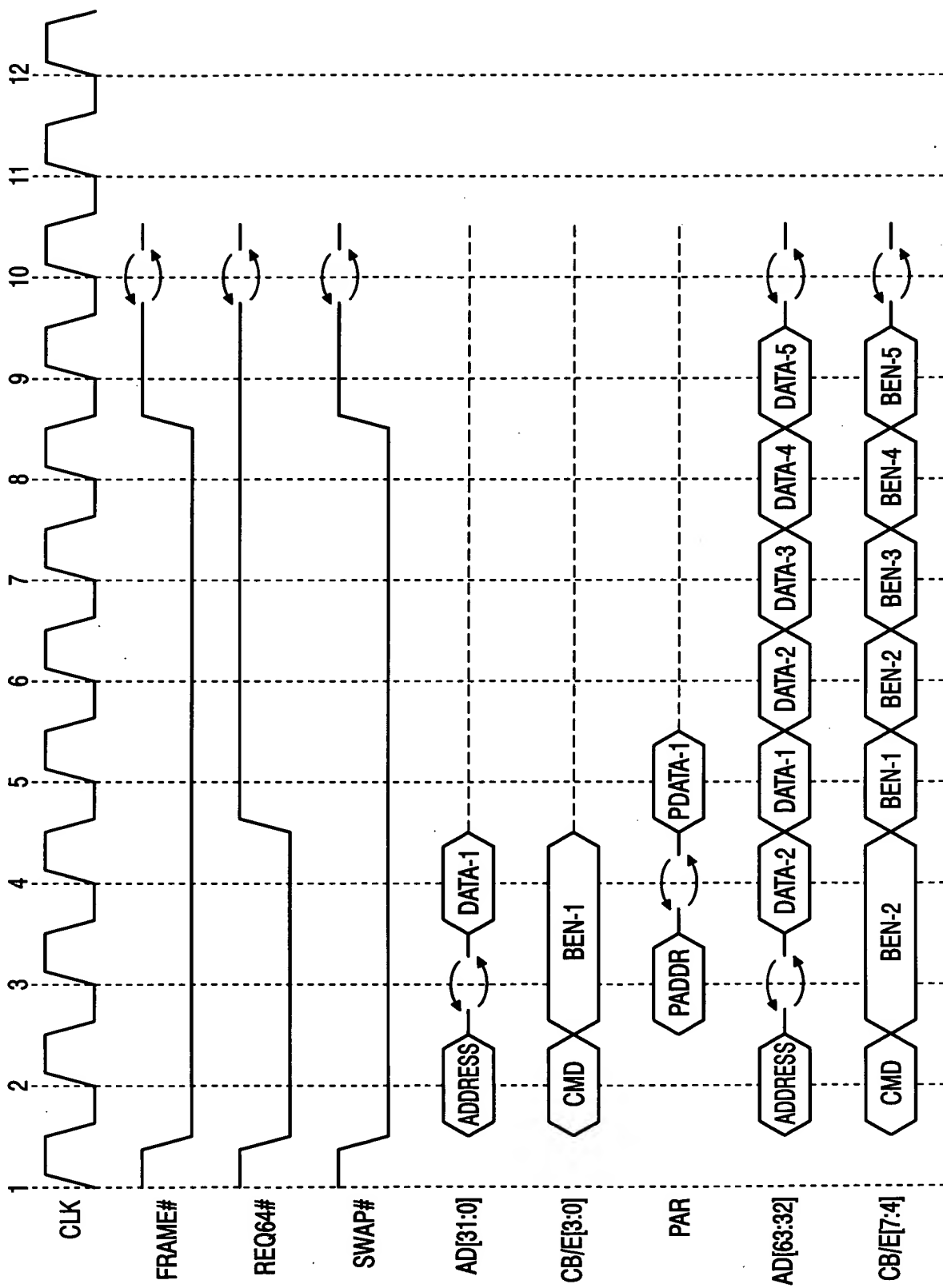


FIG. 17A

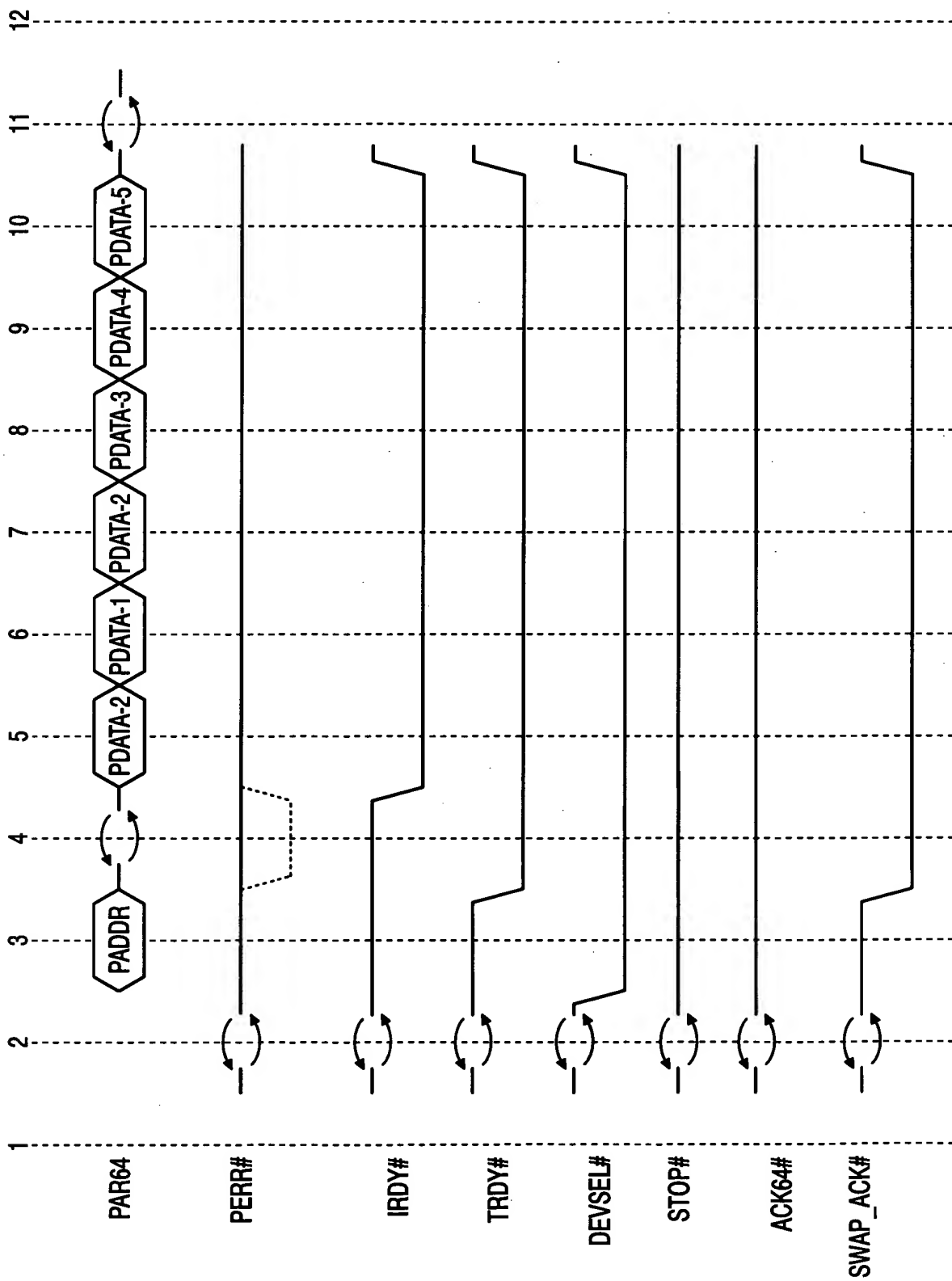


FIG. 17B

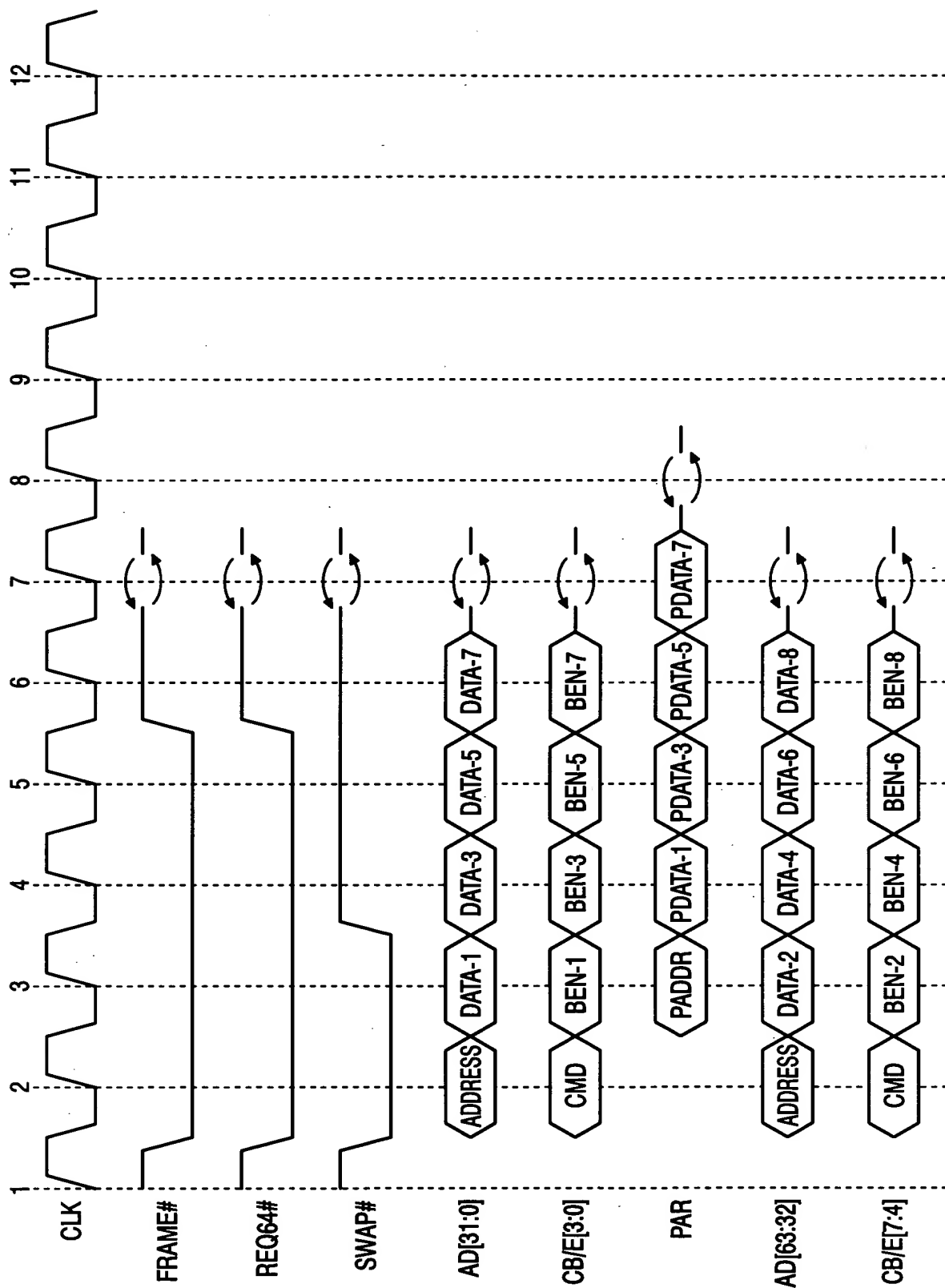


FIG. 18A

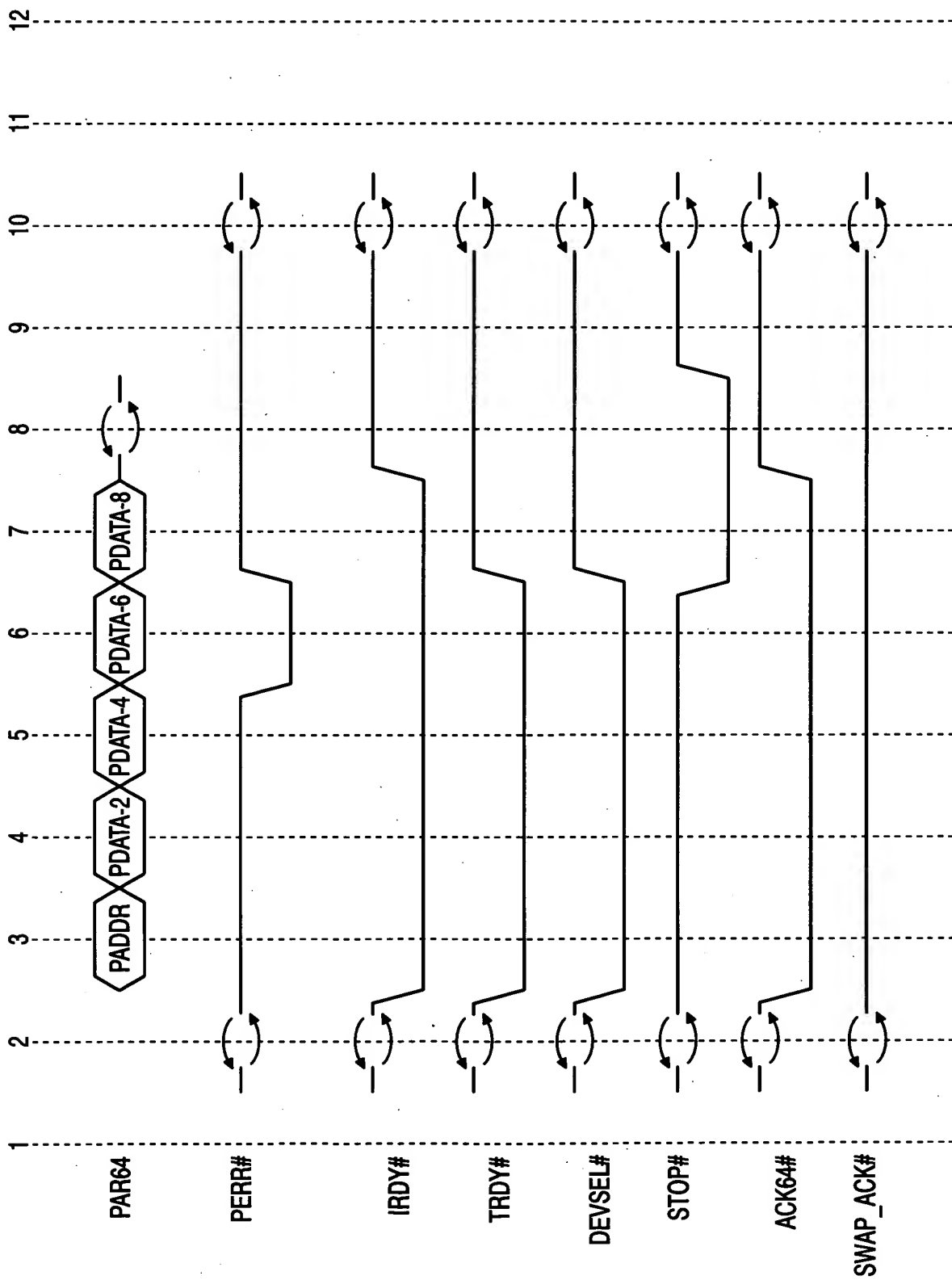


FIG. 18B



FIG. 19

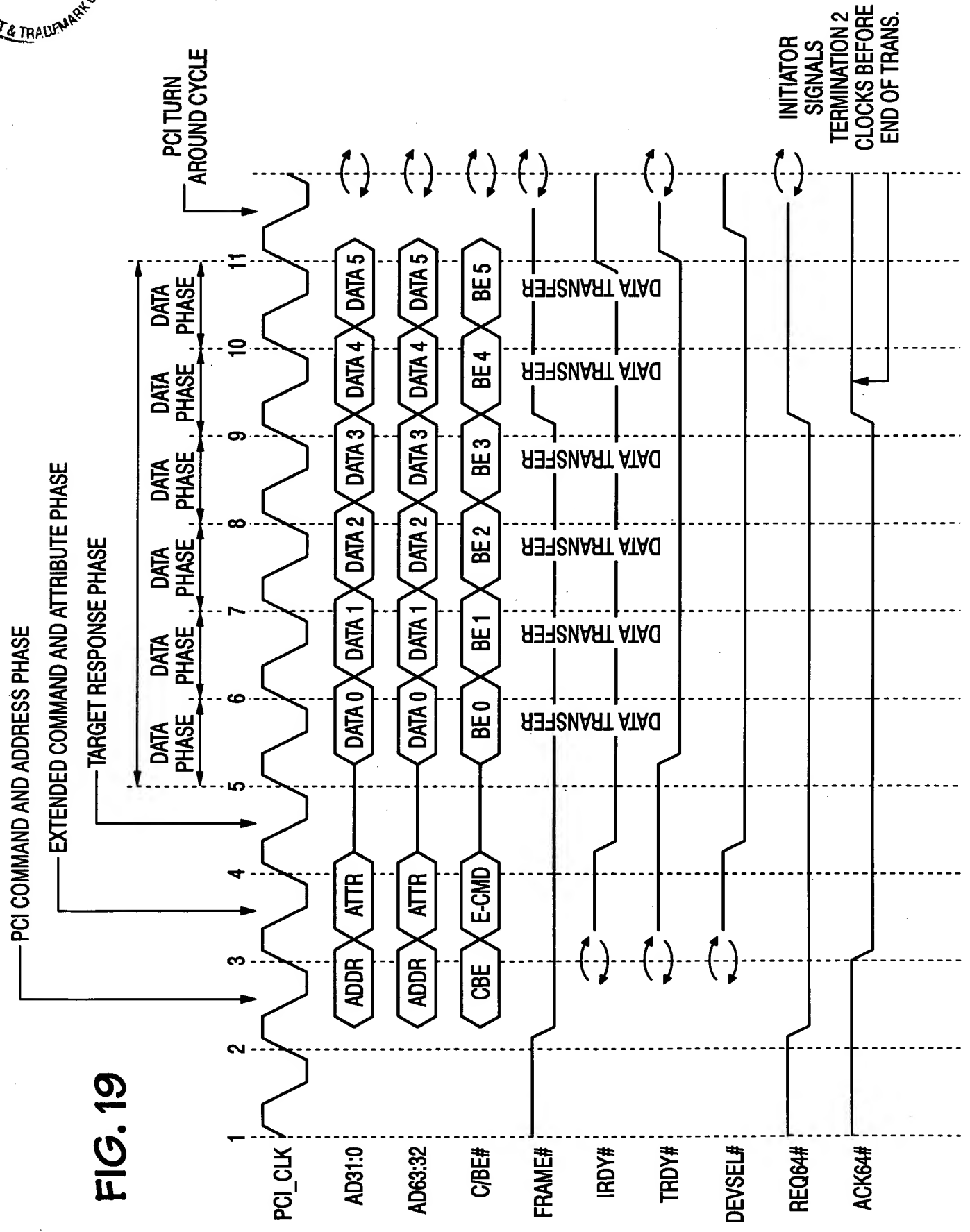


FIG. 20

